What is claimed is:

1.   A   method   for   accessing   a   frame   memory
integrated within a display panel driver driving
a display panel, said method comprising:

5   serially performing write operations for
writing sub-field data of a pixel line within
said display panel for a plurality of sub-fields
into said frame memory; and

            serially performing read operations for
10 reading sub-field data of a plurality of pixel
lines for a sub-field from said frame memory,

            wherein at least two of said write
operations are allowed to be performed between
adjacent two of said read operations.

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2.   The method according to claim 1, further
comprising:

            providing first and second horizontal sync
signals,

20   wherein said write operations for writing
said sub-field data of said pixel line for said
plurality of sub-fields are performed during a
single cycle of said first horizontal sync signal,
and

25   wherein each of said read operations for
reading said sub-field data of said pixel line
for each of said plurality of sub-fields is

performed during a single cycle of said second horizontal sync signal.

3.   The method according to claim 1, further comprising:

        providing a read request signal activated for requesting said read operations, and

        providing a write request signal activated for requesting said write operations,

        wherein, in response to activation of said read request signal, associated one of said read operations is performed immediately after said activation of said read request signal when said frame memory is not engaged in write operation, while said associated one of said read operations is performed after completion of associated one of said write operations when said frame memory is engaged in said associated one of said write operations.

4.   The method according to claim 3, wherein said read request signal is kept activated until said associated one of said read operations is initiated.

5.   The method according to claim 1, further comprising:

providing a read request signal activated
for requesting said read operations, and

providing a write request signal activated
for requesting said write operations,

5   wherein, in response to activation of said
write request signal, one of said write
operations associated with said activation is
performed immediately after said activation of
said write request signal when said frame memory
10   is not engaged in read nor write operation, said
associated one of said write operations is
performed after completion of associated one of
said read operations when said frame memory is
engaged in said associated one of said read
15   operations, and said associated one of said write
operations is performed after completion of
previous one of said write operations when said
frame memory is engaged in said previous one of
said write operations.

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6.   The method according to claim 5, wherein
said write request signal is kept activated until
said associated one of said write operations is
initiated.

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7.   A memory controller for controlling access
to a frame memory comprising:

a timing controller developing read and write start pulse signals in response to write and read request signals, and

a read/write operation control unit

5 responsive to said read and write start pulse signals for initiating read operations for reading sub-field data from said frame memory, and write operations for write sub-field data into said frame memory,

10 wherein said timing controller develops said read and write start pulse signals to allow said read/write operation control unit to initiate at least two of said write operations between adjacent two of said read operations.

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8. The memory controller according to claim 7, wherein said timing controller includes:

a state machine switching a state of said frame memory among a plurality of states in

20 response to a reset signal, said write and read request signals, said plurality of states comprising:

an idle state,

a write start state,

25 a first write operation state, and

a second write operation state,

wherein said state machine is designed to

switch said state of said frame memory to said

idle state in response to activation of said

reset signal, to switch said state of said frame

memory to said write start state in response to

5   first activation of said write request signal, to

unconditionally switch said state of said frame

memory to said first write operation state after

placing said frame memory in said write start

state to initiate one of said write operations,

10   and to switch said state of said frame memory to

said second write operation state in response to

second activation of said write request signal

during said one of said write operations to

initiate next one of said write operations.

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9.   The memory controller according to claim 8,

wherein said plurality of states further

comprising:

        a read start state, and

20   a read operation state,

        wherein said state machine is designed to

switch said state of said read start state in

response to activation of said read request

signal when said frame memory is placed in any of

25   said idle state and said first and second write

operation states, and to unconditionally switch

said state of said frame memory to said read

operation state after placing said frame memory in said read start state to initiate one of said read operations.